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EXAMINER	
ALSIP, MICHAEL	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,517	KAMIKO ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. **Claims 1, 3-13 and 16-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrel et al. (US 5,829,038) and further in view of "The Cache Memory book" by Him Handy (Handy).

2. Consider **claim 1**, Merrel et al. discloses a data processing system having: at least one processor chip including a processor unit and an internal data cache (Col. 2 lines 59-65), and an interface external to the internal data cache and which is configured to receive cache mirror data from the processor chip (where the L2-Ln part

of the cache hierarchy interfaces the main memory with the CPU and L1 cache (data cache) and receives data to be written from the processor chip), the interface further configured to discard all the cache mirror data **designated** to be written to an external memory received from the processor chip so that **the** cache mirror data **designated to be written to the external memory** is never written to the external memory during operation of the processor chip (abstract, fig. 2, Col. 3 lines 46-67 and Col. 4 lines 1-37 where the term "cache mirror data" is considered to be any portion of cached data that is received from the processor chip, but not necessarily all the cache data received from the processor chip. Also during the write-back process, cache mirror data is designated to be written back to an external memory, then a check is performed to see if a copy of the cache mirror data is found in a lower level of cache (interface) and if it is, the write-back is cancelled and the cache mirror data is evicted, therefore disclosing data the is designated to be written but then cancelled and evicted (discarded)).

Merrel does not explicitly disclose the newly added limitation wherein the interface is located outside the first processor chip. The examiner is considering the L2-Ln caches to be the interface, however in Merrel these caches happen to be integrated into the chip, however Handy (pg. 28 ¶'s 2 and 3 and table 1.1 and pg. 89-90 section 2.2.10) discloses that external caches are used in both systems that do and do not have an on-chip cache, the benefits of having additional caches being external rather than internal are reduced costs, reduced die size, and the ability to make up for some of the deficiencies of the on-chip cache, therefore being obvious to one of ordinary skill in the art.

3. Consider **claim 3**, as applied to **claim 1** above, Merrel et al. and Handy discloses a data processing system according to **claim 1** further including one or more further processing chips which have read/write access to external memory (Merrel et al.: Col. 2 lines 16-17, Col. 5 lines 22-26).

Consider **claim 4**, Merrel et al. discloses a method of operating a processing chip having a processor, an internal data cache and a cache controller for transmitting cache mirror data write instructions out of the processor chip (Col. 2 lines 60-65, Col. 3 lines 25-34), the method including discarding the write instructions **designated for an external memory** so that cache mirror data **designated to be written to the external memory** is never written to **any** external memory during the operation of the processing chip (abstract, fig. 2, Col. 3 lines 46-67 and Col. 4 lines 1-37 where the term "write instructions" is considered to be any number of write instructions that is received from the processor chip, but not necessarily all the write instructions received from the processor chip. Also during the write-back process, cache mirror data is designated to be written back to an external memory, then a check is performed to see if a copy of the cache mirror data is found in a lower level of cache (interface) and if it is, the write-back is cancelled and the cache mirror data is evicted, therefore disclosing data the is designated to be written but then cancelled and evicted (discarded)) the external interface providing a connection between the processing chip and an address controller (Fig. 1 component 60, since the memory sub-system is able to receive an address signal from the cache and use that to access and manipulate it's memory, there must be logic in the memory sub-system that controls the address information that it receives

and therefore has an address controller) and arranging for the program code operated by the processor to require only the data cache as memory (The purpose of the cache and control of the cache (replacement policy) is to reduce the amount of times the processor needs to access slower memory to retrieve its desired data by keeping as much of the require program data as possible in the cache, therefore if the program being run is only as big as the cache the program will use only the cache as its memory),

Merrel does not explicitly disclose the newly added limitation wherein the interface is located outside the first processor chip. The examiner is considering the L2-Ln caches to be the interface, however in Merrel these caches happen to be integrated into the chip, however Handy (pg. 28 ¶'s 2 and 3 and table 1.1 and pg. 89-90 section 2.2.10) discloses that external caches are used in both systems that do and do not have an on-chip cache, the benefits of having additional caches being external rather than internal are reduced costs, reduced die size, and the ability to make up for some of the deficiencies of the on-chip cache, therefore being obvious to one of ordinary skill in the art.

4. Consider **claim 5**, as applied to **claim 1** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 1**, wherein the at least one processor chip comprises exactly one processor chip (Merrel et al.: Fig. 1).

5. Consider **claim 6**, as applied to **claim 1** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 1**, wherein the at least one

processor chip comprises two processor chips (Merrel et al.: Col. 2 lines 16-17, Col. 5 lines 22-26).

6. Consider **claims 7**, as applied to **claim 1** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 1**, but does not explicitly disclose wherein the processor chip further includes an internal cache controller coupled between the internal data cache and the processor unit whereas Handy does teach this feature (Handy: Fig. 2.4 pages 42-49, all CPU/cache interactions are controlled by the cache controller which must intercept all of the CPU's signals).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the cache controller between the internal data cache and processor unit in the system of Merrel et al., because Handy teaches that all CPU/cache interactions are controlled by the cache controller which must intercept all of the CPU's signals, therefore it would be obvious for the cache controller to be between the internal data cache and processor unit (Handy: Fig. 2.4 pages 42-49).

Consider **claim 8**, Merrel et al. discloses a data processing system comprising: a processor chip including an internal processor coupled to an internal data cache (Col. 2 lines 59-65); an external memory (Fig. 1); and an interface external to the internal data cache coupled between the processor chip and the external memory, the interface configured to receive memory data from the external memory and transfer the memory data to the processor chip (where the L2-Ln part of the cache hierarchy interfaces the main memory with the CPU and L1 cache(data cache) and receives data to be written from the processor chip, the claim language does not require that the interface be

external to the processor chip, but instead that it is external to the data cache and therefore the L2-Ln part of the cache hierarchy is considered the interface between the processor and data cache combination and the external memory), the interface further configured to receive internal cache mirror data from the processor chip and discard the internal cache mirror data **designated** to be written to the external memory so that the internal cache mirror data **designated to be written to the external memory** is never written to **any** external memory (abstract, fig. 2, Col. 3 lines 46-67 and Col. 4 lines 1-37 where the term "cache mirror data" is considered to be any portion of cache data that is received from the processor chip, but not necessarily all the cache data received from the processor chip. Also during the write-back process, cache mirror data is designated to be written back to an external memory, then a check is performed to see if a copy of the cache mirror data is found in a lower level of cache (interface) and if it is, the write-back is cancelled and the cache mirror data is evicted, therefore disclosing data the is designated to be written but then cancelled and evicted (discarded)),

Merrel does not explicitly disclose the newly added limitation wherein the interface is located outside the first processor chip. The examiner is considering the L2-Ln caches to be the interface, however in Merrel these caches happen to be integrated into the chip, however Handy (pg. 28 ¶'s 2 and 3 and table 1.1 and pg. 89-90 section 2.2.10) discloses that external caches are used in both systems that do and do not have an on-chip cache, the benefits of having additional caches being external rather than internal are reduced costs, reduced die size, and the ability to make up for some of the

deficiencies of the on-chip cache, therefore being obvious to one of ordinary skill in the art.

Merrel does not explicitly disclose the newly added limitation wherein there is an address decoder, however Handy does teach the use of an address decoder (Handy: Fig. 5.5, pages 196-197) and for the limitation that the interface provides the only connection between the processor chip and the address decoder, (Merrel: fig. 1 and Handy: Fig. 5.5, pages 196-197, Handy discloses have the address decoder as part of the control circuit for the cache, which the examiner is interpreting the cache memory and its control circuitry of the L2-Ln cache of Merrel as the interface, and therefore making the interface the only connection to the address controller which is part of the interface).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have a decoder in the control circuit in the system of Merrel et al., because Handy teaches that using a decoder with the control circuit for the cache reduces delays in determining cache hits and misses (page 196-197).

7. Consider **claim 9**, as applied to **claim 8** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 8**, further comprising a control circuit coupled to the interface circuit, the control circuit providing a control signal to indicate whether data received by the interface should be discarded (the cache controllers for each cache in the hierarchy are the control circuits which contain the algorithms for determining which data is moved in and out of cache (cache replacement policy), including the eviction (discarding) of data in the cache).

8. Consider **claim 10**, as applied to **claim 9** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 9**, wherein the control circuit comprises a decoder (Handy: Fig. 5.5, pages 196-197).

9. Consider **claim 11**, as applied to **claim 8** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 8**, further comprising: a second processor chip that includes an internal processor coupled to an internal cache; and a second interface, wherein the second processor chip is coupled to the external memory through the second interface (Fig. 1, Col. 2 lines 16-17, Col. 5 lines 22-26, where each processor in the multi-processor cluster will have the same configuration as in fig. 1).

10. Consider **claim 12**, as applied to **claim 11** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 11**, further comprising a system bus coupled to the processor chip, the second processor chip, the interface, and the second interface (Fig. 1, Col. 2 lines 16-17, Col. 3 lines 24-34, Col. 5 lines 22-26, wherein in a cluster the databus will be used in the same fashion as per the embodiment described).

11. Consider **claim 13**, as applied to **claim 12** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 12**, further comprising a third processor chip coupled to the system bus (Fig. 1, Col. 2 lines 16-17, Col. 5 lines 22-26).

Consider **claim 16**, Merrel et al. discloses a method of operating a data processing system having a plurality of integrated circuits, each integrated circuit having a processor, an internal data cache, and a cache controller (Col. 2 lines 16-17 and 60-65, Col. 3 lines 25-34, Col. 5 lines 22-26), the method comprising: transmitting cache

mirror data write instructions **designated** to an external memory interface **from a first cache controller of a first integrated circuit** (Fig. 1, where the L2-Ln part of the cache hierarchy interfaces the main memory with the CPU and L1 cache(data cache) and receives data to be written from the processor chip, the cache hierarchy is considered the interface between the processor and data cache combination and the external memory); and discarding the first cache mirror data write instructions at the external memory interface so that cache mirror data **designated to be written to external memory** is never written to any external memory during operation of the first processor (abstract, fig. 2, Col. 3 lines 46-67 and Col. 4 lines 1-37 where the term "cache mirror data" is considered to be any portion of cache data that is received from the processor chip, but not necessarily all the cache data received from the processor chip. Also during the write-back process, cache mirror data is designated to be written back to an external memory, then a check is performed to see if a copy of the cache mirror data is found in a lower level of cache (interface) and if it is, the write-back is cancelled and the cache mirror data is evicted, therefore disclosing data the is designated to be written but then cancelled and evicted (discarded)).

Merrel does not explicitly disclose wherein the external memory interface is located outside the first integrated circuit. The examiner is considering the L2-Ln caches to be the interface, however in Merrel these caches happen to be integrated into the chip, however Handy (pg. 28 ¶'s 2 and 3 and table 1.1 and pg. 89-90 section 2.2.10) discloses that external caches are used in both systems that do and do not have an on-chip cache, the benefits of having additional caches being external rather than internal

are reduced costs, reduced die size, and the ability to make up for some of the deficiencies of the on-chip cache, therefore being obvious to one of ordinary skill in the art.

Consider **claim 17**, as applied to **claim 16** above, Merrel et al. in view of Brabandt and Handy disclose further comprising: transmitting second cache mirror data write instructions from a second cache controller in a second integrated circuit to the external memory interface; writing the second cache mirror data write instructions from the external memory interface to external memory (Merrel et al.: Col. 2 lines 16-17, Col. 5 lines 22-26 and Handy pg. 140 ¶ 2, where Merrel discloses a multiprocessor system and Handy discloses the ability to share the lower level caches (interface) with multiple processors and Merrel discloses the ability to write data to the external memory).

Consider **claim 18**, as applied to **claim 17** above, Merrel et al. in view of Handy disclose further comprising: determining if a task requires a read/write memory that is larger than an internal data cache size; and allocating the task to the first integrated circuit or to the second integrated circuit based upon the determining step (Brabandt abstract, the examiner considers the term "task" to only be a single instruction and the act of loading an instruction into a cache line means that it has been determined that the instruction does not need a larger memory and the act of loading also means that a circuit in the system has been allocated).

Consider **claims 19, 21, 23 and 25**, as applied to **claims 1, 4, 8 and 16** above, Merrel et al. in view of Handy disclose wherein the cache mirror data is designated to be

written to an external memory by a write Command from the at least one processor chip to the external memory (Merrell et al.: Col. 3 lines 25-45).

Consider **claims 22, 22, 24 and 26**, as applied to **claims 1, 4, 8 and 16** above, Merrel et al. in view of Handy disclose wherein the cache mirror data is designated to be written to an external memory by transmitting the cache mirror on an external interface bus coupled to the at least one processor chip and the interface (Merrell et al.: Col. 3 lines 25-45).

12. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Merrel et al. (US 5,829,038) in view of Handy as applied to **claim 1** above, and further in view of Klein (6,401,199 B1).

13. Consider **claim 2**, as applied to **claim 1** above, Merrel et al. in view of Handy disclose a data processing system according to **claim 1** in which the interface is coupled to a memory (Merrel et al: Col. 2 lines 59-65), but Merrel does not explicitly state that the interface passing data to the processor chip during initialization, whereas Klein does teach this (Klein: abstract Col. 1 lines 22-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor chip initialize through the cache hierarchy interface of Merrel, because Klein teaches that running the bootstrap programs from RAM instead of ROM is faster and also the use of ROM to hold initialization data at start-up is well-known because the data is not lost when the system is shutdown (Klein: Col. 1 lines 22-63).

14. **Claims 14 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrel et al. (US 5,829,038) in view of Handy as applied to **claim 13** above, and further in view of Stewart et al. (US 5,157,780).

15. Consider **claim 14**, as applied to **claim 13** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 13**, but does not explicitly state the system of **claim 13** wherein the third processor chip comprises a master processing unit and wherein the processor chip and the second processor chip comprise slave processing units, whereas Stewart et al. does teach this feature (Fig. 1, Col. 1 lines 13-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have a plurality of processors implemented in a master/slave configuration in the system of Merrel et al., because Stewart et al. teaches that it is common to use redundant processors to provide a fail-safe mode of operation (Col. 1 lines 13-18).

16. Consider **claim 15**, as applied to **claim 14** above, Merrel et al. in view of Handy discloses a data processing system according to **claim 14**, further comprising a second external memory directly coupled to the system bus. (The examiner is taking official notice to the fact that it is well-known and common in the art that computer systems have a type of ROM connected to the system bus for BIOS or initialization of the system upon start-up).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have a second external memory coupled to the system bus in the system of

Merrel et al., because it is notoriously well-known and common in the art to have ROM connected to the system bus to initialize a processing system upon start-up.

Response to Arguments

17. Applicant's arguments filed 5/8/2009 have been fully considered but they are not persuasive. The arguments pertaining to the newly amended claim language have been addressed in the claim language themselves above, where the claim limitation "cache mirror data designated to be written to the external memory" is being mapped to the cache mirror data of Merrell et al. where a cache line is to be evicted and is designated to be written back to main memory, but when a check is performed to see if an up to data copy of the cache mirror data is located in the lower level of cache, the write back is cancelled and the cache mirror data is evicted without it being written to any external memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Supervisory Patent Examiner, Art Unit 2186

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